HOMEWORK 4 and 5

March 15, 2009

Homework is due on Monday March 30, 2009 in Class.

Chapter 7

Answer the following questions from the Course Textbook:

7.2, 7.3, 7.4, 7.5, 7.6*, 7.7, 7.9*, 7.10*, 7.16, 7.17*, 7.18*

1. Problem from Laboratory: [This is a very important Problem which needs to be absolutely answered – This needs to go into your second report. You have sometime to answer this question.]
From Euichul (Course TA) get the predeposition and drive in conditions including ramp-up, ramp-down and steady temperature diffusion times. Based on these conditions for your wafer, calculate the expected junction depth using the analytical model. You can make your calculations more precise using temperature dependent values of $D_0$. Now use SUPREM or SENTAURUS simulation software to do the same (This can be done once Euichul gives you the details later and does not have to be submitted along with this homework). Now answer the following questions:

1. How do the results depend upon the grid size you use for your simulations?
2. Plot a profile of the concentration of phosphorus as a function of depth after predeposition and after drive in.
3. How do the numerically calculated values compare with the analytical solution?
4. Which would you like to believe? What are the main reasons for the differences between the two solutions?
7.2. A resistor is made as part of a high frequency analog integrated circuit as shown below. The N⁻ epi layer forms the body of the resistor. If the width of the resistor in the direction into the paper is 2.5μm, what should the length X be to give a resistor of approximately 50kΩ. The epilayer is doped with phosphorus at a concentration of $1 \times 10^{15}$ cm$^{-3}$ and is 3μm thick.

![Resistor Diagram]

7.3. A p-type (boron) diffusion is performed as follows:
- Pre-dep: 30 minutes, 900°C, solid solubility
- Drive-in: 60 minutes, 1000°C
(a) What is the deposited Q?
(b) If the substrate is doped $1 \times 10^{15}$ cm$^{-3}$ phosphorus, what is $x_J$.
(c) What is the sheet resistance of the diffused layer?

7.4. Suppose we perform a solid solubility limited predeposition from a doped glass source which introduces a total of Q impurities / cm².
(a) If this predeposition was performed for a total of t minutes, how long would it take (total time) to predeposit a total of 3Q impurities / cm² into a wafer if the predeposition temperature remained constant.
(b) Derive a simple expression for the $(Dt)_{drive-in}$ which would be required to drive the initial predeposition of Q impurities / cm² sufficiently deep so that the final surface concentration is equal to 1% of the solid solubility concentration. This can be expressed in terms of $(Dt)_{predep}$ and the solid solubility concentration $C_S$.

7.5. A diffused region is formed by an ultra-shallow implant followed by a drive-in. The final profile is Gaussian. Derive a simple expression for the sensitivity of $x_J$ to the implant dose Q. Is $x_J$ more sensitive to Q at high or low doses?

7.6* From a process control point of view, predeposition times > 10 min are required. From an economic point of view, times < 10 hours are required.
Equipment limitations restrict $700^\circ C < T < 1200^\circ C$. You need only consider simple Gaussian and erfc type profiles in this problem.

a). Is it possible to dope an MOS channel region by predeposition to shift threshold voltages? The required dose is $5 \times 10^{11}$ cm$^{-2}$, boron.

b). What would be a reasonable schedule $(T, t)$ for an MOS source drain predep? The required dose is $5 \times 10^{15}$ cm$^{-2}$, arsenic. The junction depth cannot be deeper than 0.2 µm for device reasons. Assume the channel doping is $1 \times 10^{18}$ cm$^{-3}$.

c). What sheet resistance would your profile in b) have if the channel doping is $1 \times 10^{18}$ cm$^{-3}$ P type?

7.7. A boron diffusion is performed in silicon such that the maximum boron concentration is $1 \times 10^{18}$ cm$^{-3}$. For what range of diffusion temperatures will electric field effects and concentration dependent diffusion coefficients be important?

7.9. A bipolar transistor is fabricated by implanting the boron base with a dose of $Q_B = 2 \times 10^{13}$ cm$^{-2}$. Then an in-situ arsenic doped polysilicon emitter region doped at $10^{20}$ cm$^{-3}$ is deposited on the surface. A drive-in is performed for 60 min at 1100$^\circ$C. Assume that the implant can be treated as a delta function. The substrate is $10^{15}$ cm$^{-3}$ N type. Calculate the base width of the final NPN bipolar transistor. You can neglect all second order effects like concentration dependent diffusion, E field effects, segregation, rapid diffusion in polysilicon etc.

7.10. A special twin-well (twin-tub) CMOS technology requires that the wells have precisely the same depth at the substrate concentration of $1 \times 10^{15}$ cm$^{-3}$, with arsenic used for the n-tub and boron used for the p-tub. A shallow implant dose of $1 \times 10^{14}$ cm$^{-2}$ is used for both and the slow diffusing arsenic is introduced first and partially driven-in. Then the boron is introduced and the rest of the anneal is performed until both junctions reach 2.5 microns. Calculate all of the drive-in times and temperatures used.

7.16 An engineer wants to use analytical solutions to diffusion equations in a programmable calculator to make rapid estimates for process changes on junction depths. Consider the following possible diffusion regimes. Which of them are most appropriate for analytical solutions (i.e. which would minimize E-field or concentration dependent effects). Explain.

7.17. A shallow phosphorus implant with a dose of $1 \times 10^{14}$ cm$^{-2}$ is covered in some regions with a deposited layer of inert nitride. An anneal is performed at 1000$^\circ$C in dry O$_2$ and a junction depth below the original surface is measured in the inert region of 0.5 µm and of 1.2 µm under the oxidizing region. What is that diffusivity enhancement that the phosphorus in the oxidizing region experiences. If $f_I$ for phosphorus is 0.9 and I-V recombination is efficient at
1000°C, what is the interstitial supersaturation that is generated by the oxidation.

7.18. Rapid Thermal Annealing (RTA) systems are becoming common for activating dopants. Silicon has quite a high thermal diffusivity of 0.88 cm² sec⁻¹, which describes how fast heat flows through silicon. Calculate the time required for a silicon wafer of thickness 500 µm to reach a constant temperature if a thin surface layer absorbs all the incident light and quickly reaches a steady state temperature of $T_s$ i.e. when does the center reach $T/T_s = 0.5$, since the wafer is heated from both sides.

CHAPTER 6: OXIDATION

Answer the following questions from the Course Textbook:

6.1, 6.3, 6.4, 6.5, 6.7, 6.8, 6.9, 6.10, 6.11, 6.12, 6.15, 6.16, 6.18, 6.19

6.1. A spherically shaped piece of silicon is cut and polished from a Czochralski single crystal ingot and oxidized in a thermal oxidation furnace. Upon pulling the silicon sphere from the furnace, the color is observed to vary significantly over the surface. Why?

6.3. An experimental MIS (I=insulator) structure is fabricated by depositing $\text{Si}_3\text{N}_4$ (silicon nitride) on a silicon substrate. The nitride is deposited by directing a jet of silane and ammonia at the surface

$$3\text{SiH}_4 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12\text{H}_2$$

A metal electrode is deposited and a C-V plot is made as shown below. A representative C-V plot is also shown for an identical structure except with thermally grown $\text{SiO}_2$ as the insulator. Explain the lateral shift in the C-V curve of the $\text{Si}_3\text{N}_4$.

6.4. Construct a HF CV plot for a P-type silicon sample, analogous to Fig. 6-9. Explain your plot based on the behavior of holes and electrons in the semiconductor in a similar manner to the discussion in the text for Fig. 6.9.
6.5. A MOS structure is fabricated to make C-V measurements as shown below. The C-V plot shows the result if the P⁺ diffusion is NOT present. Sketch the expected shape of the C-V plot with the P⁺ diffusion. Explain.

6.7. Why is steam oxidation more rapid than dry O₂ oxidation?

6.8. Under what conditions is the thermal growth rate of SiO₂ linearly proportional to time?

6.9. According to the Deal Grove model, oxidation kinetics start out linear and become parabolic as the oxidation proceeds. Calculate the oxide thickness at which this transition takes place and plot this versus oxidation temperature.

6.10. Does the oxide thickness at which there is a transition from linear to parabolic rates change if we perform an oxidation at a pressure of 20 atmospheres rather than at 1 atmosphere.

6.11. A MOS device requires a gate oxide of 10nm ± 0.5nm. Assume the growth is done at 900°C in dry O₂. Neglect any effect of the anomalous initial growth. Derive a simple expression which gives the sensitivity of the oxide thickness to growth temperature \( dx/dT \). Evaluate this expression to see how well controlled the furnace T must be in order to obtain 10nm ± 0.5nm at 900°C.

6.12 A silicon wafer is covered by an SiO₂ film 0.3 μm thick.
   a. What is the time required to increase the thickness by 0.5 μm by oxidation in H₂O at 1200°C?
   b. Repeat for oxidation in dry O₂ at 1200°C.

6.15. The structure shown below is formed by oxidizing a silicon wafer \( x_0 = 200 \) nm, and then using standard masking and etching techniques to remove the SiO₂ in the center region. An N⁺ doping step is then used to produce the structure shown. The structure is next placed in an oxidation furnace and oxidized at 900°C in H₂O. The oxide will grow faster over the N⁺ region than it will over the lightly doped substrate. Assume that B/A is enhanced by 4X over the N⁺ region. Will the growing oxide over the N⁺ region ever catch up in thickness to the other oxide? If so, when and at what thickness. Use the Deal Grove model for the oxidation kinetics.
6.16. A 1µm wide trench is etched in a <100> silicon wafer, so that the sides of the trench are <110> planes. An angled implant is performed, doping the sidewall N+ and thereby enhancing the linear rate constant by a factor of 4. The structure is then oxidized in steam at 1100°C. At what time during the oxidation will the groove be filled with SiO2? Assume the appropriate oxidation coefficients scale as [ (111 : 110 : 100) = (1.68 : 1.2 : 1.0) ].

6.18. Silicon on Insulator or SOI is a new substrate material that is being considered for future integrated circuits. The structure, shown below, consists of a thin single crystal silicon layer on an insulating (SiO2) substrate. The silicon below the SiO2 provides mechanical support for the structure. One of the reasons this type of material is being considered, is because junctions can be diffused completely through the thin silicon layer to the underlying SiO2. This reduces junction capacitances and produces faster circuits. Isolation is also easy to achieve in this material, because the thin Si layer can be completely oxidized, resulting in devices completely surrounded by SiO2. A LOCOS process is used to locally oxidize through the silicon as shown on the right below. Assuming the LOCOS oxidation is done in H2O at 1000°C, how long will it take to oxidize through the 0.3 µm silicon layer? Calculate a numerical answer using the Deal Grove model.
6.19. As MOS devices are scaled to smaller dimensions, gate oxides must be reduced in thickness. a). As the gate oxide thickness decreases, do MOS devices become more or less sensitive to sodium contamination? Explain. b). As the gate oxide thickness decreases, what must be done to the substrate doping (or alternatively the channel $V_{TH}$ implant, to maintain the same $V_{TH}$?