Features
- Available in SC-70-5 and SOT-23-5 packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I\text{Q} = 100 \ \mu A \ (typical)
- Phase Margin: 90° (typical)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual and Quad Packages

Applications
- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids
- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Description
The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typical). It also maintains 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100 µA (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of \(V_{DD} + 300 \text{ mV}\) to \(V_{SS} - 300 \text{ mV}\). This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 6.0V.

Typical Application

\[ \text{Gain} = 1 + \frac{R_1}{R_2} \]

Non-Inverting Amplifier
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

- $V_{DD} - V_{SS} \leq 7.0\text{V}$
- Current at Analog Input Pins ($V_{IN+}, V_{IN-}$) $\leq \pm 2\text{mA}$
- Analog Inputs ($V_{IN+}, V_{IN-}$) $\leq V_{SS} - 1.0\text{V}$ to $V_{DD} + 1.0\text{V}$
- All Other Inputs and Outputs $\leq V_{SS} - 0.3\text{V}$ to $V_{DD} + 0.3\text{V}$
- Difference Input Voltage $\leq |V_{DD} - V_{SS}|$
- Output Short Circuit Current Continuous
- Current at Output and Supply Pins $\leq \pm 30\text{mA}$
- Storage Temperature $-65°C$ to $+150°C$
- Maximum Junction Temperature ($T_J$) $+150°C$
- ESD Protection On All Pins (HBM; MM) $\geq 4\text{kV}$

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{k}\Omega$ to $V_L$, and $V_{OUT} = V_{DD}/2$ (refer to Figure 1-1 and Figure 1-2).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset</td>
<td>$V_{OS}$</td>
<td>-4.5</td>
<td>---</td>
<td>+4.5</td>
<td>mV</td>
<td>$V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Input Offset Drift with Temperature $\Delta V_{OS}/\Delta T_A$</td>
<td>---</td>
<td>±2.0</td>
<td>---</td>
<td>---</td>
<td>µV/°C</td>
<td>$T_A = -40°C$ to $+125°C$, $V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>---</td>
<td>86</td>
<td>---</td>
<td>dB</td>
<td>$V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>Input Bias Current and Impedance</td>
<td>$I_B$</td>
<td>---</td>
<td>±1.0</td>
<td>---</td>
<td>pA</td>
<td>$T_A = +85°C$</td>
</tr>
<tr>
<td>Industrial Temperature</td>
<td>$I_B$</td>
<td>---</td>
<td>19</td>
<td>---</td>
<td>pA</td>
<td>$T_A = +85°C$</td>
</tr>
<tr>
<td>Extended Temperature</td>
<td>$I_B$</td>
<td>---</td>
<td>1100</td>
<td>---</td>
<td>pA</td>
<td>$T_A = +125°C$</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>---</td>
<td>±1.0</td>
<td>---</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Common Mode Input Impedance</td>
<td>$Z_{CM}$</td>
<td>---</td>
<td>$10^{13}</td>
<td>\Omega</td>
<td>6$</td>
<td>---</td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>$Z_{DIFF}$</td>
<td>---</td>
<td>$10^{13}</td>
<td>\Omega</td>
<td>3$</td>
<td>---</td>
</tr>
<tr>
<td>Common Mode</td>
<td>$V_{CMR}$</td>
<td>$V_{SS} - 0.3$</td>
<td>---</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
<td>$V_{CM} = -0.3\text{V}$ to $5.3\text{V}$, $V_{DD} = 5\text{V}$</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>CMRR</td>
<td>60</td>
<td>76</td>
<td>---</td>
<td>dB</td>
<td>$V_{OUT} = 0.3\text{V}$ to $V_{DD} - 0.3\text{V}$, $V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>DC Open-Loop Gain (Large Signal)</td>
<td>$A_{OL}$</td>
<td>88</td>
<td>112</td>
<td>---</td>
<td>dB</td>
<td>$V_{OUT} = 0.3\text{V}$ to $V_{DD} - 0.3\text{V}$, $V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>Output</td>
<td>$V_{OL}, V_{OH}$</td>
<td>$V_{SS} + 25$</td>
<td>---</td>
<td>$V_{DD} - 25$</td>
<td>mV</td>
<td>$V_{DD} = 5.5\text{V}$, $0.5\text{V}$ Input Overdrive</td>
</tr>
<tr>
<td>Maximum Output Voltage Swing</td>
<td>$I_{SC}$</td>
<td>---</td>
<td>±6</td>
<td>---</td>
<td>mA</td>
<td>$V_{DD} = 1.8\text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>---</td>
<td>±23</td>
<td>---</td>
<td>mA</td>
<td>$V_{DD} = 5.5\text{V}$</td>
</tr>
<tr>
<td>Output Short Circuit Current</td>
<td>$I_{Q}$</td>
<td>50</td>
<td>100</td>
<td>170</td>
<td>µA</td>
<td>$I_{Q} = 0$, $V_{DD} = 5.5\text{V}$, $V_{CM} = 5\text{V}$</td>
</tr>
</tbody>
</table>

Note 1: MCP6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

Note 2: All parts with date codes November 2007 and later have been screened to ensure operation at $V_{DD} = 6.0\text{V}$. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.
1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-1 and Figure 1-2. The bypass capacitors are laid out according to the rules discussed in Section 4.4 “Supply Bypass”.

FIGURE 1-1: AC and DC Test Circuit for Most Non-Inverting Gain Conditions.

FIGURE 1-2: AC and DC Test Circuit for Most Inverting Gain Conditions.
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, TA = +25°C, VDD = +1.8V to +5.5V, VSS = GND, VCM = VDD/2, VOUT ≈ VDD/2, VL = VDD/2, RL = 10 kΩ to VL, and CL = 60 pF.

FIGURE 2-1: Input Offset Voltage.

FIGURE 2-2: Input Offset Voltage Drift.

FIGURE 2-3: Input Offset Quadratic Temp. Co.

FIGURE 2-4: Input Offset Voltage vs. Common Mode Input Voltage at VDD = 1.8V.

FIGURE 2-5: Input Offset Voltage vs. Common Mode Input Voltage at VDD = 5.5V.

FIGURE 2-6: Input Offset Voltage vs. Output Voltage.
Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\ \text{k}\Omega$ to $V_L$, and $C_L = 60\ \text{pF}$.

**FIGURE 2-7:** Input Bias Current at $+85^\circ\text{C}$.

**FIGURE 2-8:** Input Bias Current at $+125^\circ\text{C}$.

**FIGURE 2-9:** CMRR, PSRR vs. Ambient Temperature.

**FIGURE 2-10:** PSRR, CMRR vs. Frequency.

**FIGURE 2-11:** Open-Loop Gain, Phase vs. Frequency.

**FIGURE 2-12:** Input Noise Voltage Density vs. Frequency.
**Note:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k} \Omega$ to $V_L$, and $C_L = 60 \text{ pF}$.

**FIGURE 2-13:** Output Short Circuit Current vs. Power Supply Voltage.

**FIGURE 2-14:** Output Voltage Headroom vs. Output Current Magnitude.

**FIGURE 2-15:** Quiescent Current vs. Power Supply Voltage.

**FIGURE 2-16:** Small-Signal, Non-Inverting Pulse Response.

**FIGURE 2-17:** Large-Signal, Non-Inverting Pulse Response.

**FIGURE 2-18:** Slew Rate vs. Ambient Temperature.
**Note:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, and $C_L = 60 \, pF$.

**FIGURE 2-19:** Output Voltage Swing vs. Frequency.

**FIGURE 2-20:** Measured Input Current vs. Input Voltage (below $V_{SS}$).

**FIGURE 2-21:** The MCP6001/2/4 Show No Phase Reversal.
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT, VOUTA</td>
<td>Analog Output (op amp A)</td>
</tr>
<tr>
<td>VIN–, VIN+</td>
<td>Inverting Input (op amp A)</td>
</tr>
<tr>
<td>VIN+*</td>
<td>Non-inverting Input (op amp A)</td>
</tr>
<tr>
<td>VDD</td>
<td>Positive Power Supply</td>
</tr>
<tr>
<td>VIN–*</td>
<td>Inverting Input (op amp B)</td>
</tr>
<tr>
<td>VIN+*</td>
<td>Non-inverting Input (op amp B)</td>
</tr>
<tr>
<td>VOUTB</td>
<td>Analog Output (op amp B)</td>
</tr>
<tr>
<td>VOUTC</td>
<td>Analog Output (op amp C)</td>
</tr>
<tr>
<td>VIND–, VIND+</td>
<td>Inverting Input (op amp D)</td>
</tr>
<tr>
<td>VINC–, VINC+</td>
<td>Non-inverting Input (op amp D)</td>
</tr>
<tr>
<td>VSS</td>
<td>Negative Power Supply</td>
</tr>
<tr>
<td>VOUTD</td>
<td>Analog Output (op amp D)</td>
</tr>
</tbody>
</table>

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (VDD) is 1.8V to 6.0V higher than the negative power supply (VSS). For normal operation, the other pins are at voltages between VSS and VDD.

Typically, these parts are used in a single (positive) supply configuration. In this case, VSS is connected to ground and VDD is connected to the supply. VDD will need bypass capacitors.
4.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip’s state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6001/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-21 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_b). The input ESD diodes clamp the inputs when they try to go more than one diode drop below VSS. They also clamp any voltages that go too far above VDD; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

![FIGURE 4-1: Simplified Analog Input ESD Structures.](image1)

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the VIN+ and VIN− pins (see Absolute Maximum Ratings † at the beginning of Section 1.0 “Electrical Characteristics”). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (VIN+ and VIN−) from going too far below ground, and the resistors R1 and R2 limit the possible current drawn out of the input pins. Diodes D1 and D2 prevent the input pins (VIN+ and VIN−) from going too far above VDD, and dump any currents onto VDD. When implemented as shown, resistors R1 and R2 also limit the current through D1 and D2.

![FIGURE 4-2: Protecting the Analog Inputs.](image2)

It is also possible to connect the diodes to the left of resistors R1 and R2. In this case, current through the diodes D1 and D2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (VIN+ and VIN−) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (VCM) is below ground (VSS); see Figure 2-20. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6001/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (VCM), while the other operates at high VCM. With this topology, the device operates with VCM up to 0.3V above VDD and 0.3V below VSS.

The transition between the two input stages occurs when VCM = VDD – 1.1V. For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amps is VDD – 25 mV (minimum) and VSS + 25 mV (maximum) when RL = 10 kΩ is connected to VDD/2 and VDD = 5.5V. Refer to Figure 2-14 for more information.
4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

![Figure 4-3: Output resistor, R_{ISO} stabilizes large capacitive loads.](image)

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance \(\frac{C_L}{G_N}\), where \(G_N\) is the circuit’s noise gain. For non-inverting gains, \(G_N\) and the Signal Gain are equal. For inverting gains, \(G_N\) is \(1+|\text{Signal Gain}|\) (e.g., -1 V/V gives \(G_N = +2\) V/V).

![Figure 4-4: Recommended R_{ISO} values for Capacitive Loads.](image)

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (VDD for single-supply) should have a local bypass capacitor (i.e., 0.01 \(\mu\)F to 0.1 \(\mu\)F) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 \(\mu\)F or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6004) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

![Figure 4-5: Unused Op Amps.](image)

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is \(10^{12}\Omega\). A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6001/1R/1U/2/4 family’s bias current at 25°C (typically 1 pA).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.
1. **Non-inverting Gain and Unity-Gain Buffer:**
   a. Connect the non-inverting pin (V\textsubscript{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V\textsubscript{IN}-). This biases the guard ring to the common mode input voltage.

2. **Inverting Gain and Transimpedance Gain Amplifiers** (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V\textsubscript{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V\textsubscript{DD}/2 or ground).
   b. Connect the inverting pin (V\textsubscript{IN}-) to the input with a wire that does not touch the PCB surface.

### 4.7 Application Circuits

#### 4.7.1 **UNITY-GAIN BUFFER**

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-7.

#### 4.7.2 **ACTIVE LOW-PASS FILTER**

The MCP6001/2/4 op amp’s low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100X the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10X higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-8 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10X higher than the cutoff frequency. The component values were selected using Microchip’s FilterLab® software.
4.7.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. **Figure 4-9** shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in **Figure 4-9**.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C₁ is sampled to C₂ for a sample time defined by tSAMPLE. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, C₁ discharges through R₁ for a time defined by tCLEAR. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V_IN on C₁ for a time defined by tDETECT.

In order to define tSAMPLE and tCLEAR, it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R₁ (τ = R₁C₁). tDETECT is the time that the input signal is sampled on C₁ and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C₁ and C₂), could create slewing limitations as the input voltage (V_IN) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short circuit current of I_SC = 25 mA and a load capacitor of C₁ = 0.1 µF, then:

\[
\frac{dV_{C1}}{dt} = I_SC \cdot C_1
\]

\[
\frac{dV_{C1}}{dt} = \frac{I_SC}{C_1} = \frac{25mA}{0.1 \mu F} = 250mV/\mu s
\]

This voltage rate of change is less than the MCP6001/2/4 slew rate of 0.6 V/µs. When the input voltage swings below the voltage across C₁, D₁ becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 µF capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40 µF and a stabilizing resistor (RISO) needs to be properly selected. (Refer to Section 4.3 “Capacitive Loads”).

**FIGURE 4-9:** Peak Detector with Clear and Sample CMOS Analog Switches.
5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6001/1R/1U/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6001/1R/1U/2/4 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip’s FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip’s product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user’s guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- P/N SOIC8EV: 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board
- P/N SOIC14EV: 14-Pin SOIC/TSSOP/DIP Evaluation Board

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: “Select the Right Operational Amplifier for your Filtering Circuits”, DS21821
AN722: “Operational Amplifier Topologies and DC Specifications”, DS00722
AN723: “Operational Amplifier AC Specifications and Applications”, DS00723
AN884: “Driving Capacitive Loads With Op Amps”, DS00884
AN990: “Analog Sensor Conditioning Circuits – An Overview”, DS00990

These application notes and others are listed in the design guide:
“Signal Chain Design Guide”, DS21825
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

5-Lead SC-70 (MCP6001)

XXN (Front)
YWW (Back)

Example: (I-Temp)

Device | I-Temp Code | E-Temp Code
-------|-------------|------------
MCP6001 | AAN         | CDN        |

Note: Applies to 5-Lead SC-70.

5-Lead SOT-23 (MCP6001/1R/1U)

XXNN

Example: (E-Temp)

Device | I-Temp Code | E-Temp Code
-------|-------------|------------
MCP6001 | AANN        | CDNN       |
MCP6001R| ADNN        | CENN       |
MCP6001U| AFNN        | CFNN       |

Note: Applies to 5-Lead SC-70.

8-Lead PDIP (300 mil)

Example:

MCP6002
I/P256

0432

Note: Applies to 5-Lead SOT-23.

Legend:

- **XX...X** Customer-specific information
- **Y** Year code (last digit of calendar year)
- **YY** Year code (last 2 digits of calendar year)
- **WW** Week code (week of January 1 is week ‘01’)
- **NNN** Alphanumeric traceability code
- **@3** Pb-free JEDEC designator for Matte Tin (Sn)
- **\*** This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Package Marking Information (Continued)

8-Lead SOIC (150 mil)

Example:

14-Lead PDIP (300 mil) (MCP6004)

Example:

8-Lead MSOP

Example:

14-Lead SOIC (150 mil) (MCP6004)

Example:

14-Lead TSSOP (MCP6004)

Example:
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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<tbody>
<tr>
<td>Dimension Limits</td>
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<tr>
<td>Number of Pins</td>
<td>N</td>
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<tr>
<td>Pitch</td>
<td>e</td>
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<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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<td>Lead Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

### WCSP Package Dimensions

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
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<tbody>
<tr>
<td><strong>Dimension Limits</strong></td>
<td><strong>MIN</strong></td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Overall Row Spacing §</td>
<td>eB</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

---

Microchip Technology Drawing C04-018B
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
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<td>Molded Package Thickness</td>
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</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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### RECOMMENDED LAND PATTERN

---

<table>
<thead>
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<td>Dimension</td>
<td>Limits</td>
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<td>Contact Pitch</td>
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<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
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<tr>
<td>Contact Pad Width (X1)</td>
<td>X1</td>
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<tr>
<td>Contact Pad Length (X1)</td>
<td>Y1</td>
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**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
2. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
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<th>Units</th>
<th>MILLIMETERS</th>
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<td>Dimension Limits</td>
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<td>Number of Pins</td>
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<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B
14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dimension Limits</strong></td>
<td><strong>MIN</strong></td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Overall Row Spacing §</td>
<td>eB</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B
14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

<table>
<thead>
<tr>
<th>Units</th>
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<tr>
<td>Pitch</td>
<td>e</td>
<td>1.27 BSC</td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>–</td>
<td>1.75</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>1.25</td>
<td>–</td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
<td>0.10</td>
<td>–</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>6.00 BSC</td>
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<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>3.90 BSC</td>
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<tr>
<td>Overall Length</td>
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<td>8.65 BSC</td>
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<td>Chamfer (optional)</td>
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<td>Foot Length</td>
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<td>–</td>
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<td>Lead Thickness</td>
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<td>Mold Draft Angle Top</td>
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<td>–</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
<td>5°</td>
<td>–</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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<tbody>
<tr>
<td><strong>Dimension Limits</strong></td>
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<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
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<tr>
<td>Molded Package Length</td>
<td>D</td>
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<td>Foot Length</td>
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<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B
APPENDIX A: REVISION HISTORY

Revision H (May 2008)
The following is the list of modifications:
1. **Design Aids**: Name change for Mindi Simulation Tool.
2. **Package Types**: Correct device labeling error.
3. **Section 1.0 “Electrical Characteristics”, DC Electrical Specifications**: Changed “Maximum Output Voltage Swing” condition from 0.9V Input Overdrive to 0.5V Input Overdrive.
4. **Section 1.0 “Electrical Characteristics”, AC Electrical Specifications**: Changed Phase Margin condition from G = +1 to G= +1 V/V.
5. **Section 5.0 “Design AIDS”**: Name change for Mindi Simulation Tool.

Revision G (November 2007)
The following is the list of modifications:
1. Updated notes to **Section 1.0 “Electrical Characteristics”**.
2. Increased Absolute Maximum Voltage range at input pins.
3. Increased maximum operating supply voltage ($V_{DD}$).
4. Added test circuits.
5. Added Figure 2-3 and Figure 2-20.
6. Added **Section 4.1.1 “Phase Reversal”, Section 4.1.2 “Input Voltage and Current Limits”, Section 4.1.2 “Input Voltage and Current Limits” and Section 4.5 “Unused Op Amps”**.
7. Updated **Section 5.0 “Design AIDS”**.
8. Updated **Section 6.0 “Packaging Information”**

Revision F (March 2005)
The following is the list of modifications:
1. Updated **Section 6.0 “Packaging Information”** to include old and new packaging examples.

Revision E (December 2004)
The following is the list of modifications:
1. $V_{OS}$ specification reduced to ±4.5 mV from ±7.0 mV for parts starting with date code YYWW = 0449
2. Corrected package markings in **Section 6.0 “Packaging Information”**.
3. Added Appendix A: Revision History.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>/XX</th>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP6001T:</td>
<td></td>
<td></td>
<td>Single Op Amp (Tape and Reel)</td>
<td></td>
<td>LT = Plastic Package (SC-70), 5-lead (MCP6001 only)</td>
</tr>
<tr>
<td>MCP6001RT:</td>
<td></td>
<td></td>
<td>Single Op Amp (Tape and Reel) (SOT-23)</td>
<td></td>
<td>OT = Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6001, MCP6001R, MCP6001U)</td>
</tr>
<tr>
<td>MCP6001UT:</td>
<td></td>
<td></td>
<td>Single Op Amp (Tape and Reel) (SOT-23)</td>
<td></td>
<td>MS = Plastic MSOP, 8-lead</td>
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<tr>
<td>MCP6002:</td>
<td></td>
<td></td>
<td>Dual Op Amp</td>
<td></td>
<td>P = Plastic DIP (300 mil body), 8-lead, 14-lead</td>
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<tr>
<td>MCP6002T:</td>
<td></td>
<td></td>
<td>Quad Op Amp (Tape and Reel)</td>
<td></td>
<td>SN = Plastic SOIC, (3.99 mm body), 8-lead</td>
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<td>MCP6004:</td>
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<td>Quad Op Amp (Tape and Reel) (SOIC, MSOP)</td>
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<td>SL = Plastic SOIC (3.99 body), 14-lead</td>
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<tr>
<td>MCP6004T:</td>
<td></td>
<td></td>
<td>Quad Op Amp (Tape and Reel) (SOIC, MSOP)</td>
<td></td>
<td>ST = Plastic TSSOP (4.4mm body), 14-lead</td>
</tr>
</tbody>
</table>

Temperature Range: I = -40°C to +85°C  
                   E = -40°C to +125°C

Examples:

a) MCP6001T-I/LT: Tape and Reel, Industrial Temperature, 5LD SC-70 package
b) MCP6001T-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
c) MCP6001RT-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
d) MCP6001UT-E/OT: Tape and Reel, Extended Temperature, 5LD SOT-23 package.
e) MCP6002-I/MS: Industrial Temperature, 8LD MSOP package.
f) MCP6002-I/P: Industrial Temperature, 8LD PDIP package.
g) MCP6002-E/P: Extended Temperature, 8LD PDIP package.
h) MCP6002-I/SN: Industrial Temperature, 8LD SOIC package.
i) MCP6002T-I/MS: Tape and Reel, Industrial Temperature, 8LD MSOP package.
j) MCP6004-I/P: Industrial Temperature, 14LD PDIP package.
k) MCP6004-I/SL: Industrial Temperature, 14LD SOIC package.
l) MCP6004-E/SL: Extended Temperature, 14LD SOIC package.
m) MCP6004-I/ST: Industrial Temperature, 14LD TSSOP package.
n) MCP6004T-I/SL: Tape and Reel, Industrial Temperature, 14LD SOIC package.
o) MCP6004T-I/ST: Tape and Reel, Industrial Temperature, 14LD TSSOP package.
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