# COURSE SYLLABUS

***CMPEN 271/275 - Fall 2016***

**Instructor**: K. Dudeck
**Office** : L-104
**Hours** : Posted outside office,
additional hours by appointment.
**Phone** : 450-3085 **Email**: ked2@psu.edu

**Reference Text**: Marcovitz, A., Introduction to Logic Design,
Prentice Hall Inc., Third Ed. 2010. (Optional)

CMPEN 271 (3:3:0) **Introduction to Digital Systems**, Introduction to logic design and digital systems. Boolean algebra, and introduction to combinatorial and sequential circuit design and analysis.
CMPEN 275 (1:0:2) **Digital Design Laboratory,** Introduction to digital design techniques.

**Grading**: The grading is broken down between lecture and lab components.

| CMPEN 271 (Lecture) | | CMPEN 275 (Lab) | |
|---|---|---|---|
| (3+3) Quizzes | 100 pts | Participation | 25pts |
| Exam I | 100 pts | 2 Quizzes | 50pts |
| Exam II | 100 pts | Lab Reports | 100pts |
| Final | 100 pts | Project | 25pts |
| Total | **400 pts** | Total | **200pts** |

**Grade cutoffs**: These are the total points needed for each letter Grade
CMPEN 271: ( A: 360, B+: 348, B: 320, C+: 308, C: 280, D: 240 )
CMPEN 275: ( A: 180, B+: 174, B: 160, C+: 154, C: 140, D: 120 )

**Policies:**

- Dates and content of exams and quizzes will be announced at least one week in advance. Students are expected to notify me 24 hours prior to a quiz or exam absence.
- Academic integrity is expected. See next page for policy.
- Class attendance is vital to successful performance on exams.
- Attendance in lab is mandatory. Lab work can NOT be made up.
- Lab reports are due one week after the lab. A 2 point per day penalty will be applied for late lab reports or assignments.
- Participation Grade is determined by attendance, completion of lab objectives, and respect of lab and lab equipment.

- **Homework**: Assigned reading will further advance comprehension of lectures and is expected to be completed by the beginning of the next class. Assigned homework problems are expected to be completed after each lecture, prior to the next class. Problems will be covered in a problem session class which will occur approximately every other week.

- The complete list of reading assignments and homework problems are given on tentative course outline.

Academic Integrity at Penn State : A Statement by the Council of Academic Deans

Academic integrity mandates the pursuit of teaching, learning, research, and creative activity in an open, honest, and responsible manner. An academic community that values integrity promotes the highest levels of personal honesty, respect for the rights, property, and dignity of others, and fosters an environment in which students and scholars can enjoy the fruits of their efforts. Academic integrity includes a commitment neither to engage in acts of falsification, misrepresentation, or deception, nor to tolerate such acts by other members of the community.

Academic integrity is a fundamental value at Penn State. It must be at the heart of all our endeavors and must guide our actions every day as students and as members of the faculty, administration, and staff. Because we expect new and continuing members of the University community to meet the high standards that are the foundation of a Penn State education, this message must be clear and reinforced frequently.

The primary responsibility for supporting and promoting academic integrity lies with the faculty and administration, but students must be active participants. A climate of integrity is created and sustained through ongoing conversations about honesty, trust, fairness, respect, and responsibility and the embodiment of these values in the life of the University. Students and faculty should contribute actively to fostering a climate of academic integrity in all their scholarly activities, through discussions in first-year seminars and in other courses, and through involvement in college Academic Integrity Committees. The University community should be continually mindful of the need to preserve academic integrity even as technology changes methods of information access and use.

Colleges will provide all faculty members and teaching assistants information about appropriate ways to promote academic integrity and handle dishonesty cases. Faculty members and graduate assistants must make clear their expectations about academic integrity in every course they teach.

As members of the Council of Academic Deans, we strongly support efforts to enhance academic integrity at Penn State. We will provide individual and collective leadership to strengthen further the University's commitment to the highest standards of academic integrity.
August 29, 2000

| Class | CMPEN 271 Topic | Text | Problems |
|---|---|---|---|
| > 1 | Number Systems | 1.2 | 1.4-**1** |
| 2 | Base Conversions | 1.2.1 | 1.4-**2,3,4** |
| 3 | Arithmetic Operations | 1.2.2 | 1.4-**5** |
| > 4 | Digital Circuits | 2.2, 2.6 | 2.11-3 |
| 5 | Boolean Algebra | 2.2,3,7 | 2.11-4**,5,8,10,11** |
| 6 | Conical Forms | 2.3,4,5 | 2.11-13**,14** |
| > 7 | 2 and 3 Variable K-maps | 3.1 | 3.8-1a,e, 2**a,b,c** |
| 8 | HOMEWORK / QUIZ 1 | - | - |
| 9 | 4 Variable K-maps | 3.1,2 | 3.8-2**e-k** |
| > 10 | Complements and K-maps | 3.3,4,5 ,6 | 3.8-5**a-c,7a-d** |
| 11 | NAND & NOR Logic | 2.10 | 2.11-**26** |
| 12 | XOR & XNOR Logic | | |
| > 13 | Negative Binary Numbers | 1.2.3 | 1.4-**6,7,8** |
| 14 | Signed Complements | 1.2.4 | 1.4-**9,10** |
| 15 | Combinational Circuits | 2.1 | 2.11-2**b,h,k,** |
| > 16 | Combinational Design | 5..8.1,3 | 1.4-**12,13** |
| 17 | HOMEWORK/REVIEW | | **5.10-25** |
| 18 | <OPEN> | | |
| > 19 | EXAM I | | |
| 20 | Arithmetic Circuits | 5.1 | 5.10-**3,4** |
| 21 | Programmable Logic | 5.6 | 5.10-**15c,21c** |
| 22 | Decoders & ROM | 5.2,3 | 5.10-**7,8** |
| > 23 | Multiplexers | 5.4 | 5.10-**13,14** |
| 24 | HOMEWORK / QUIZ 2 | - | |
| 25 | Hardware Language (VHDL) | 5.7 | |
| 26 | Sequential Logic | 6.1 | 6.6-2 |
| > 27 | Flip Flops | 6.3 | 6.6-**3,4** |
| 28 | Sequential Analysis | 6.4 | 6.6 -5**,1** |
| 29 | State Table/Diagram | | 6.6-**8** |
| > 30 | Sequential Design (D) | 7.1,2 | 7.6-3**(i),7(i)** |
| 31 | Sequential Design (J-K) | 7.3 | 7.6-3**(ii),9** |
| 32 | HOMEWORK/REVIEW | | |
| > 33 | <OPEN> | | |
| 34 | EXAM II | | |
| 35 | Moore/Mealy Machines | 7.4 | 7.6-**15** |
| > 36 | Registers | 8.1 | |
| 37 | Shift Registers | | 810-**1,4** |
| 38 | Counters - Asynchronous | 8.2 | 8.9- **7** |
| > 39 | Counters - Synchronous | 8.7 | 8.9- **9,12(a,c)** |
| 40 | Counter Stability | | |
| 41 | HOMEWORK / QUIZ 3 | | |
| > 42 | RAM | Sup | |
| 43 | Memory Systems | Sup | |
| 44 | <OPEN> | | |
| 45 | REVIEW | | |

CMPEN 275 Laboratory Experiments

| **Week** | **Lab Experiment** | **Assignment** |
|---|---|---|
| 1 | Orientation | |
| 2 | #1 - Oscilloscope | |
| 3 | #2 - Binary Numbers | Lab Quiz 1 |
| 4 | #3 - The Binary Inverter | Report |
| 5 | #4 - Digital I/O | |
| 6 | #5 - Combinational Analysis | Lab Quiz 2 |
| 7 | <OPEN> | |
| 8 | #6 - Combinational Design | Report |
| 9 | #7 -BCD to Seven Seg Display | |
| 10 | Sup. Lab #1 - Field Programmable Logic Devices (FPLD)and VHDL | |
| 11 | #10 – Clocks and Pulse | |
| 12 | #9-1 - Sequential Design – Part 1 | |
| 13 | #9-2 - Sequential Design – Part 2 | |
| 14 | Project | |
| 15 | Project | Presentation and Report |